Figure 1

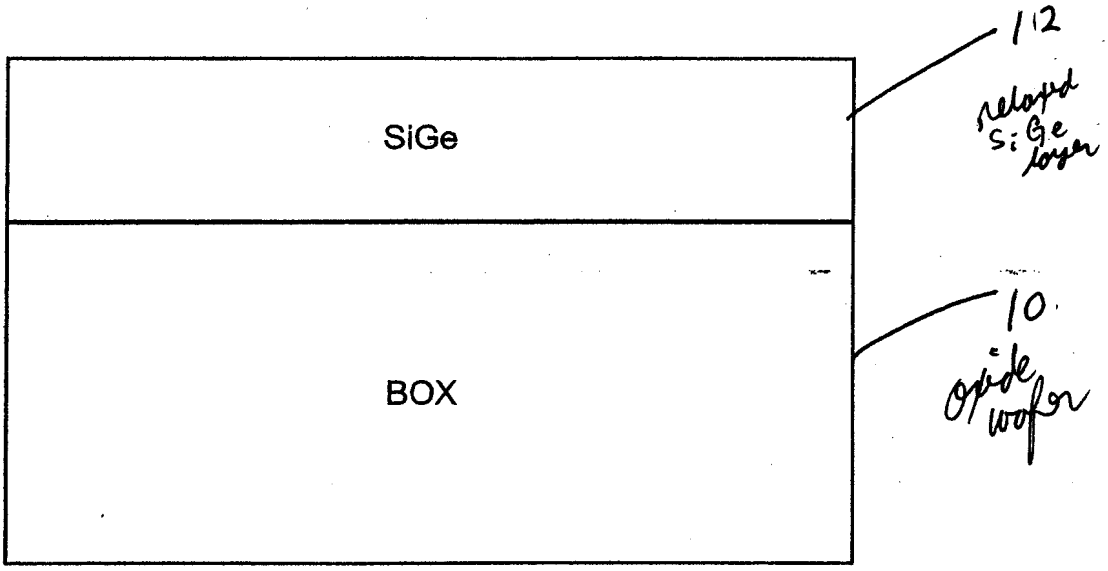


Figure 2

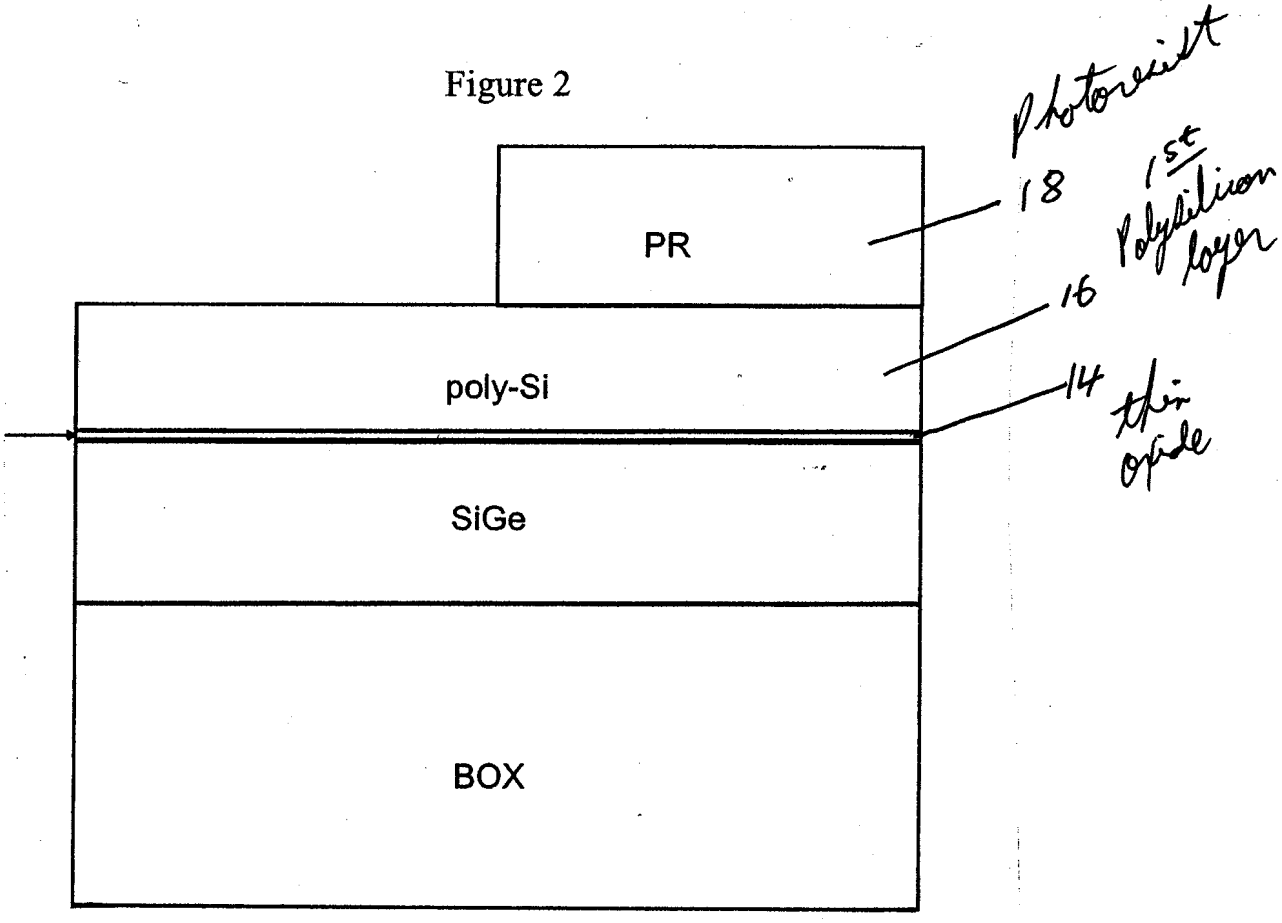
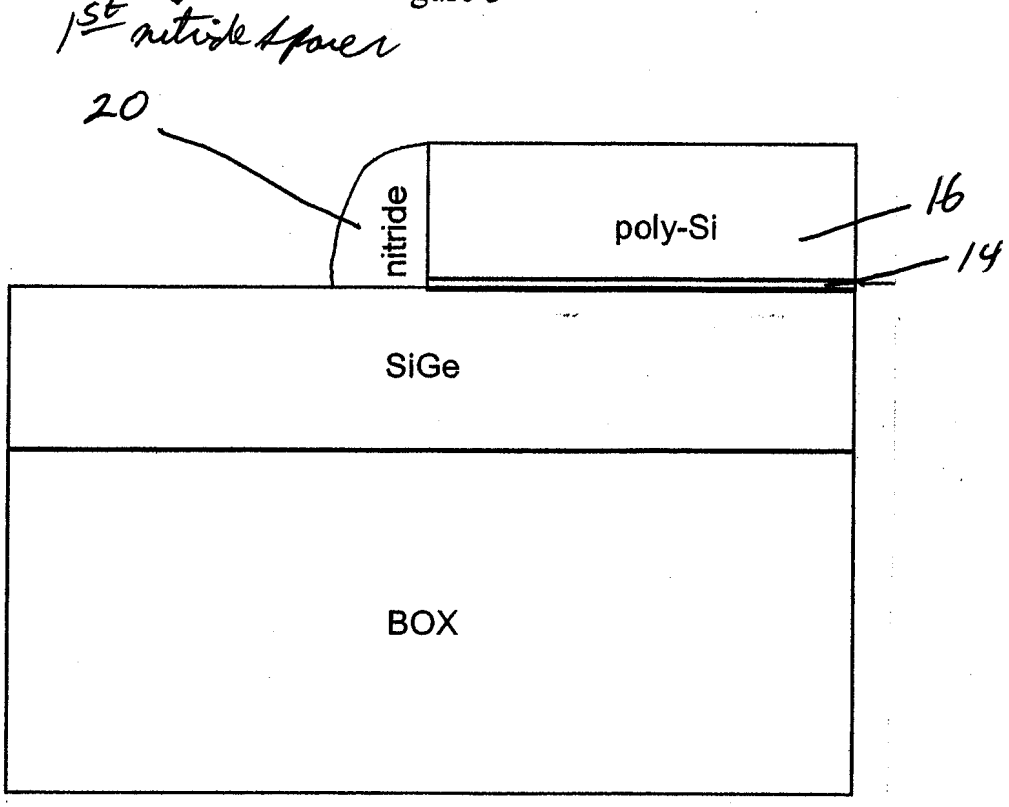


Figure 3



2nd nitride spacer

Figure 4

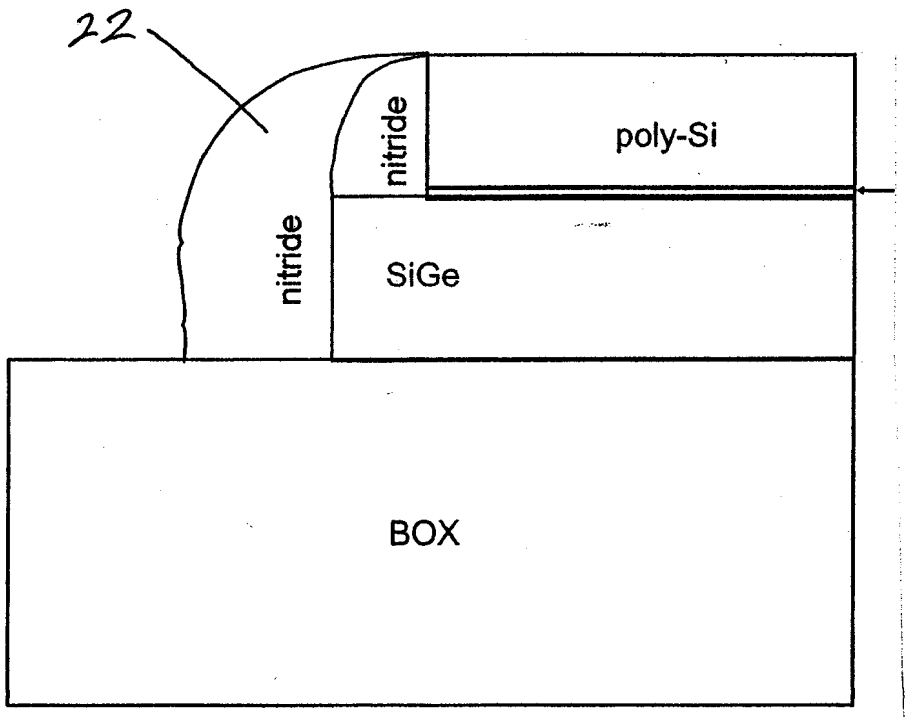


Figure 5

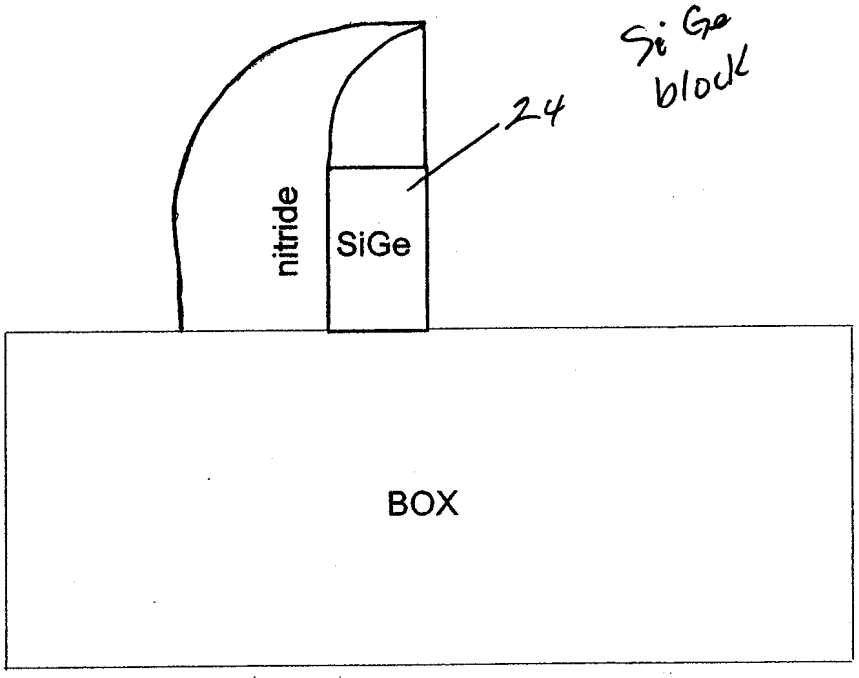


Figure 6

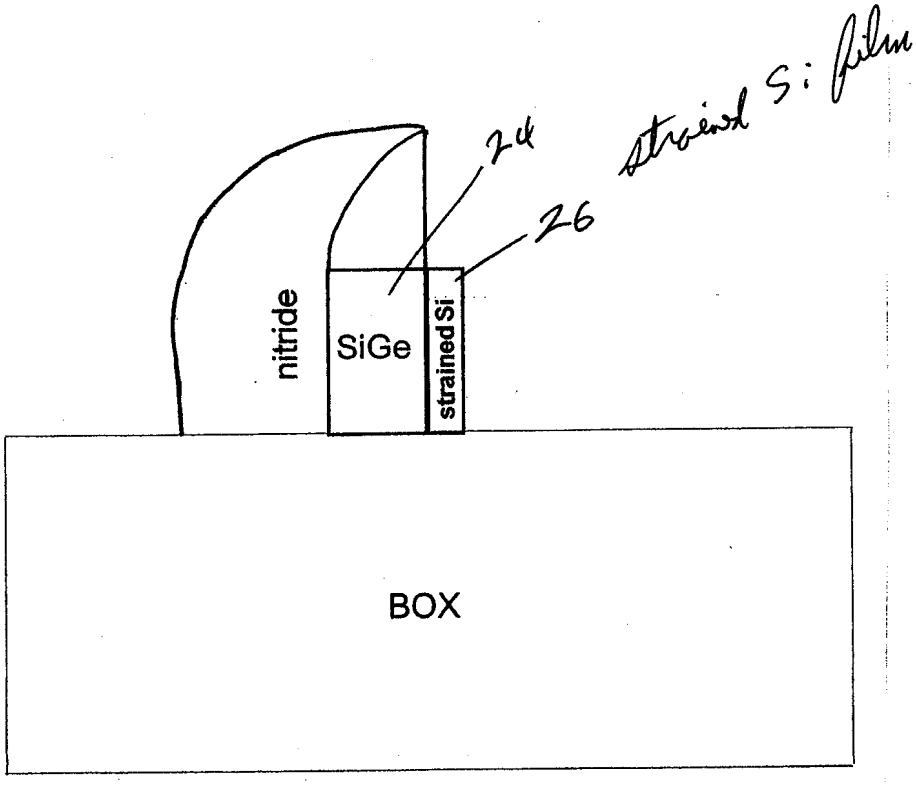


Figure 7

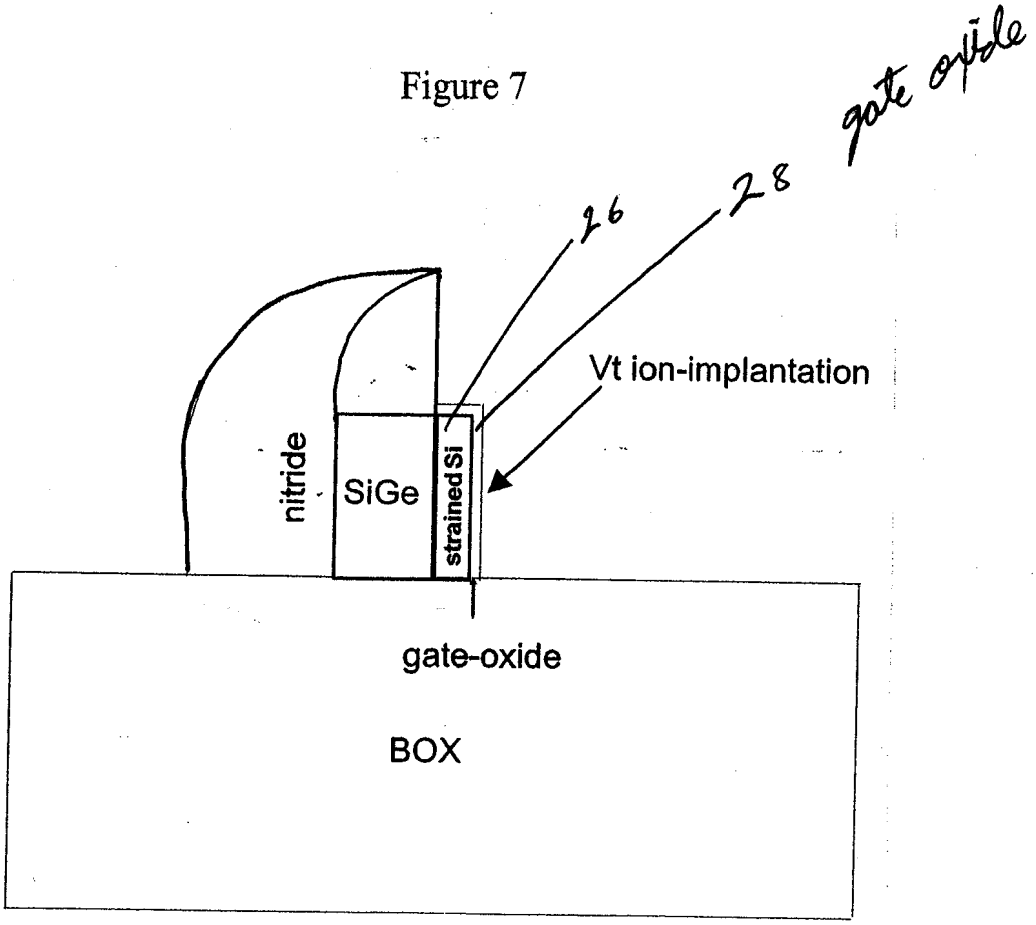
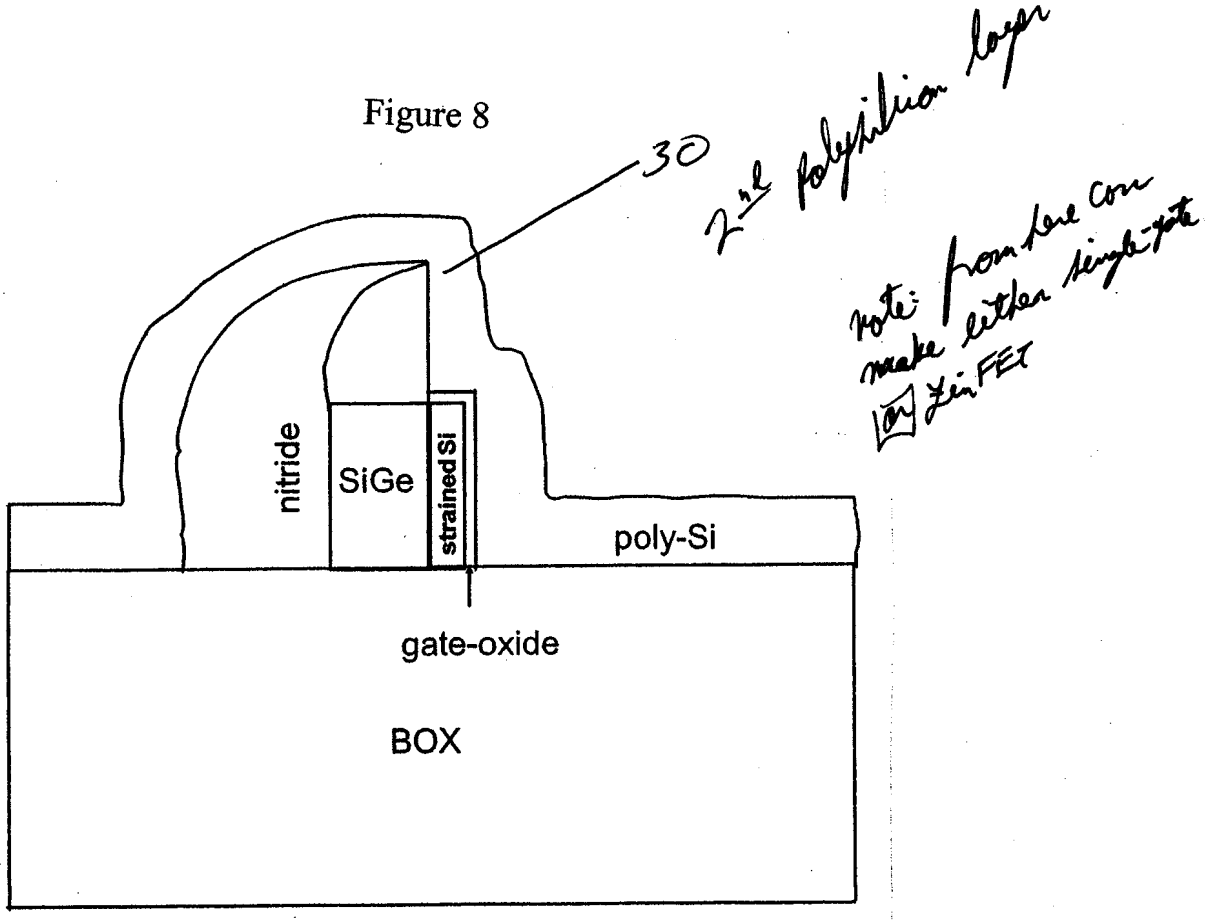


Figure 8



single gate device

Figure 9

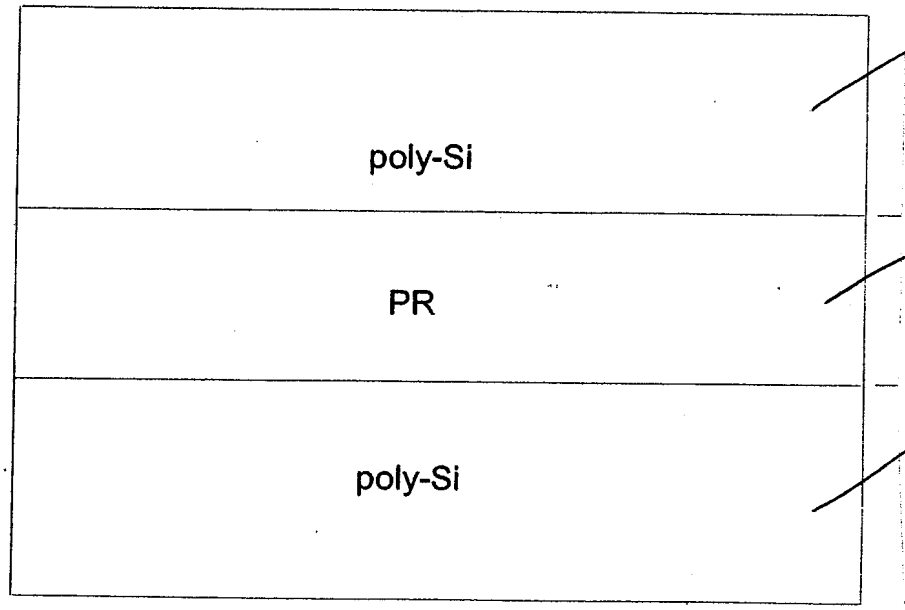


Figure 10

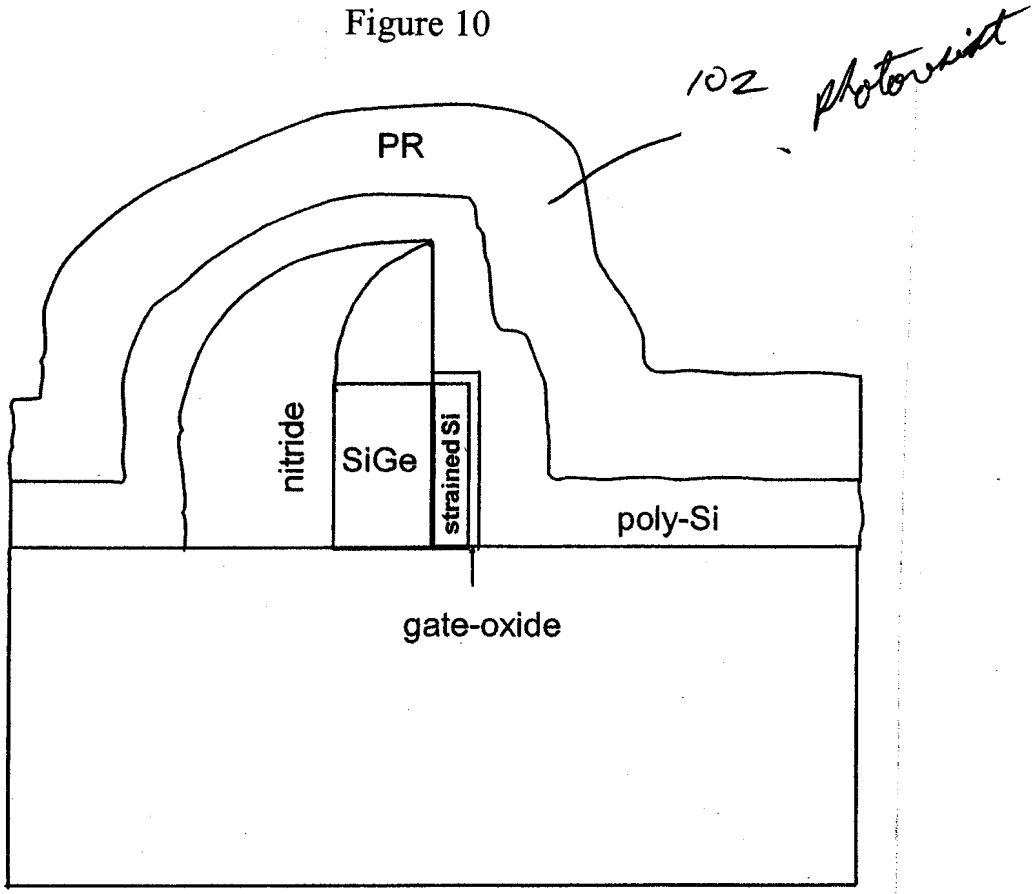
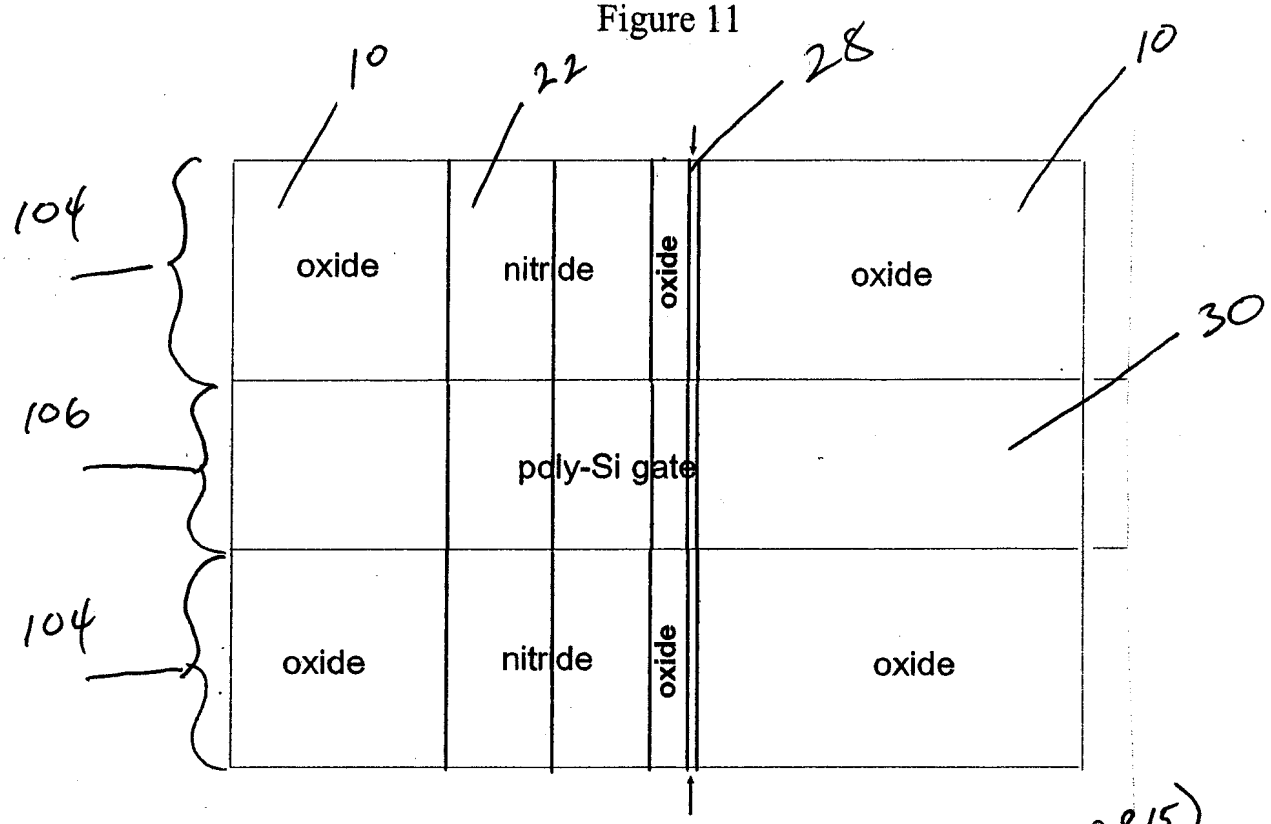


Figure 11



~~Figure 12~~ (same as Fig 8&15)

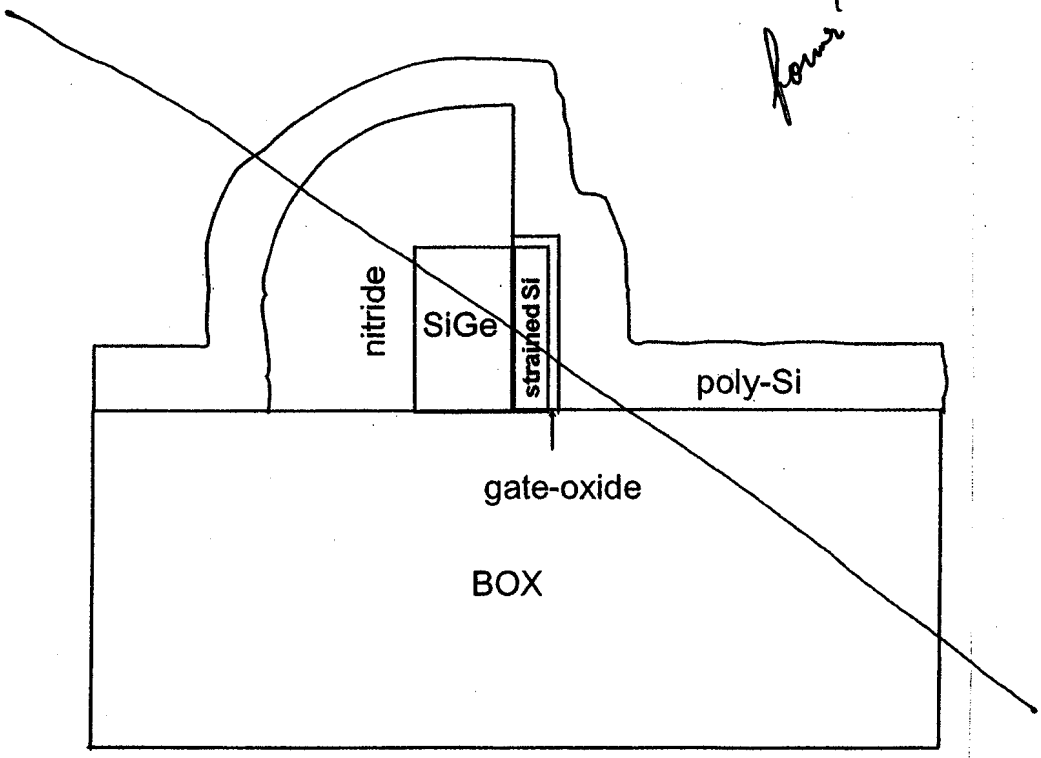


Figure 12

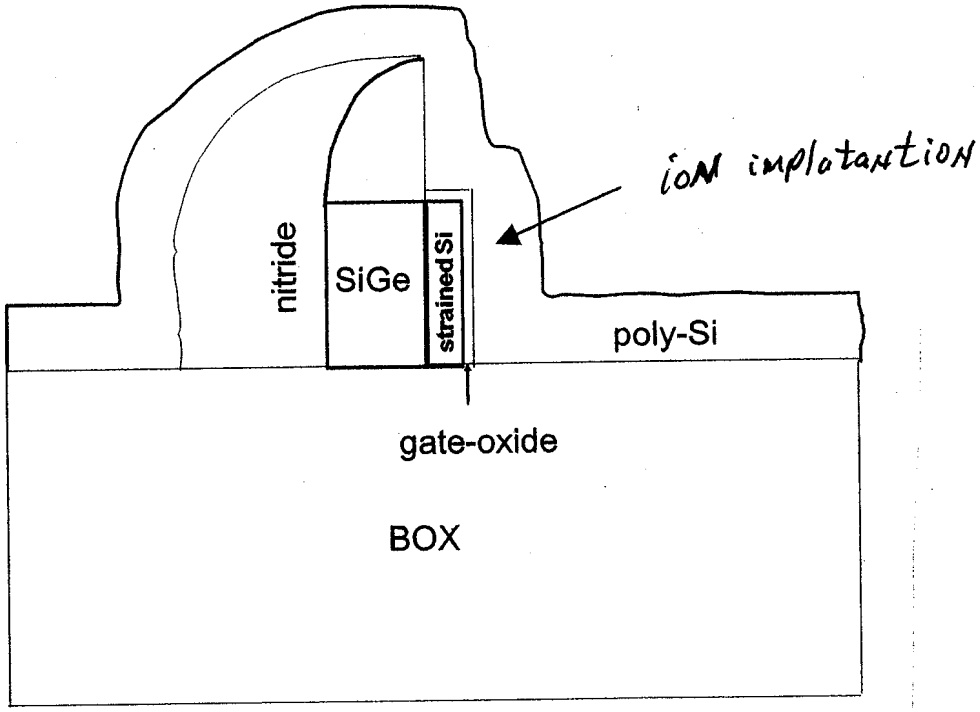


Figure 13

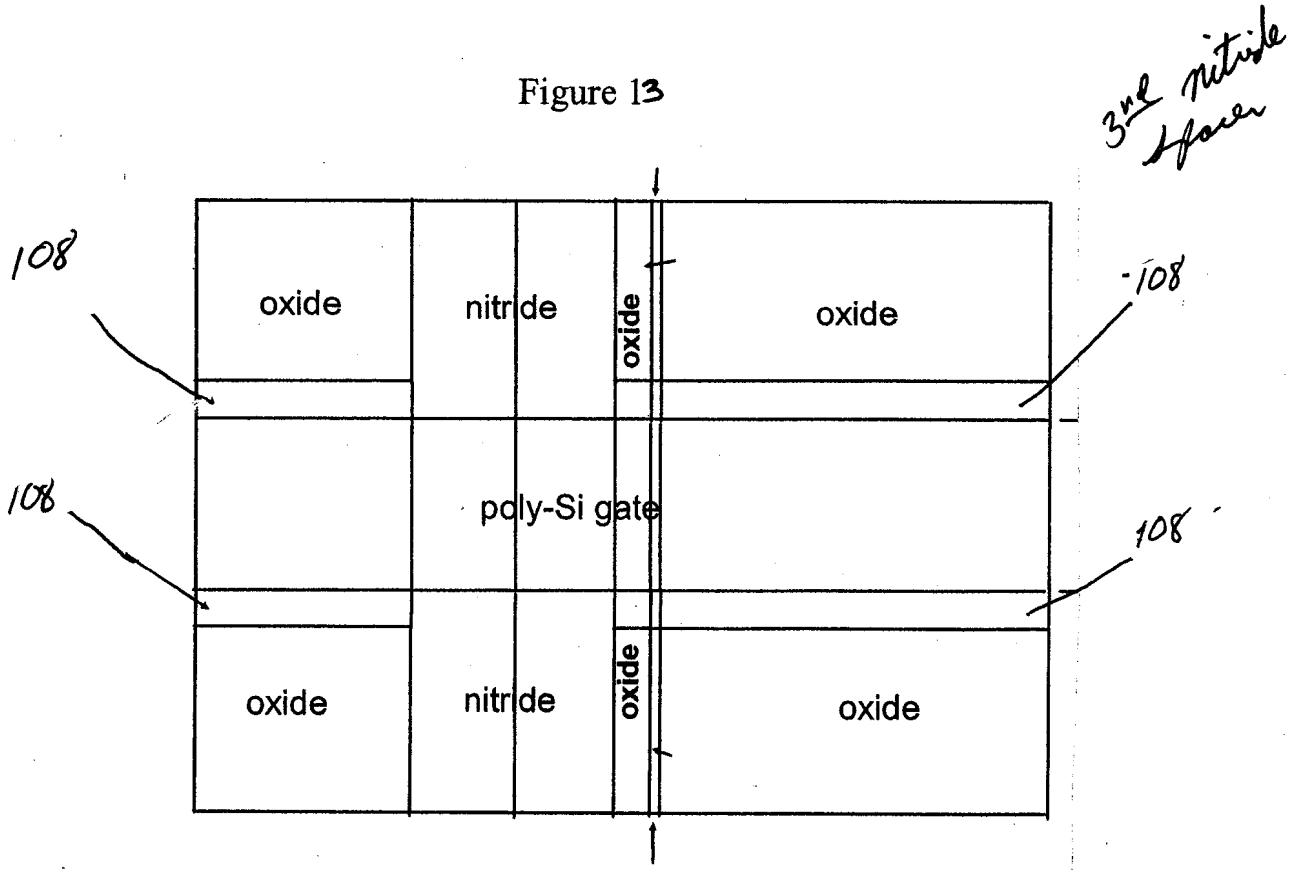
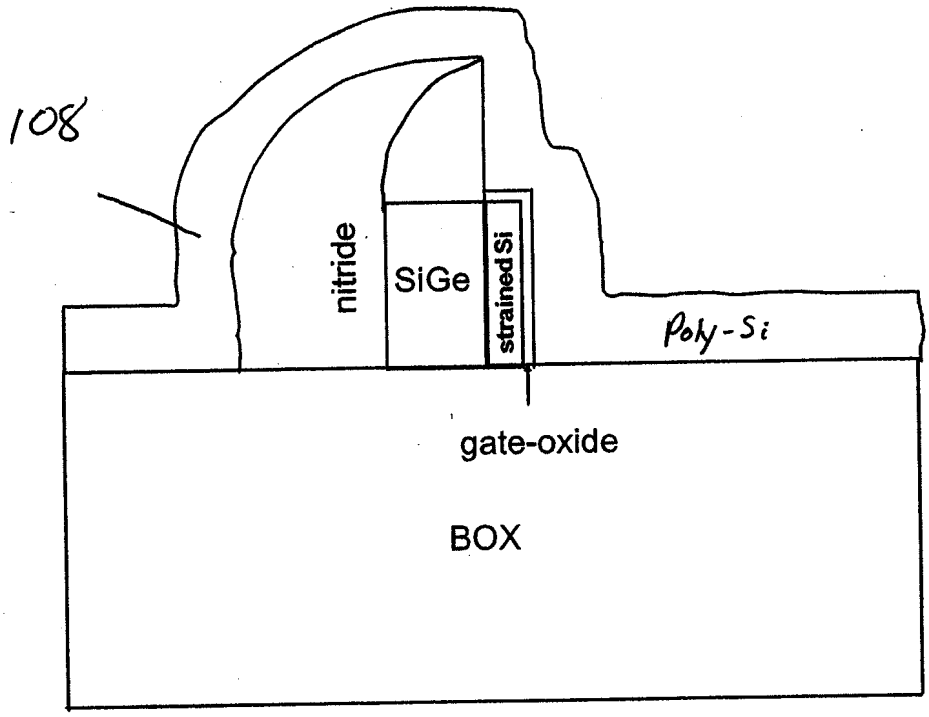


Figure 14



Single-gate device

Figure 15

double-gate FinFET

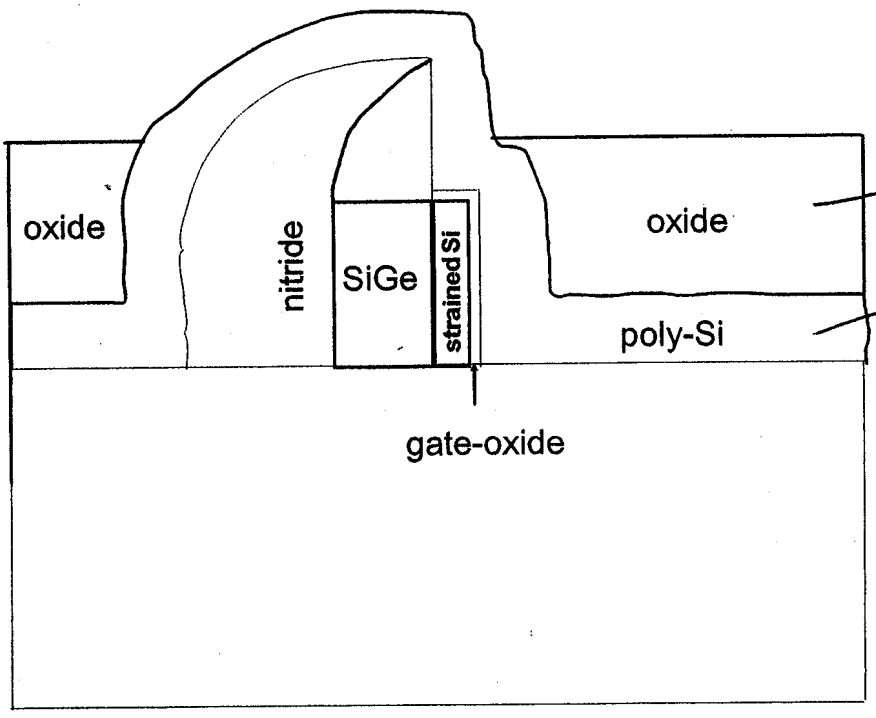


Figure 16

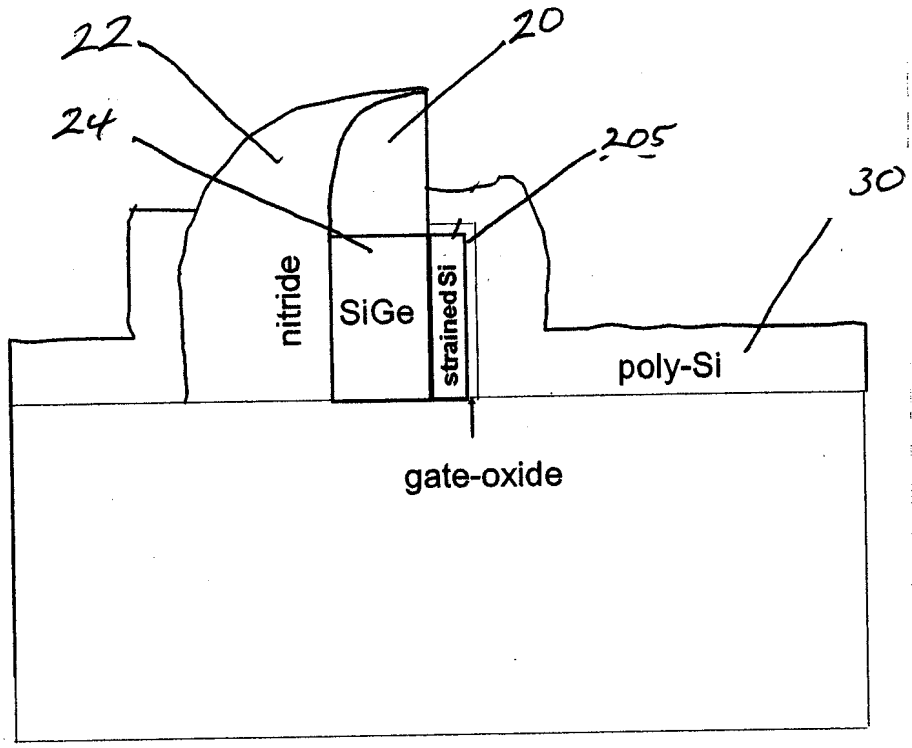


Figure 17

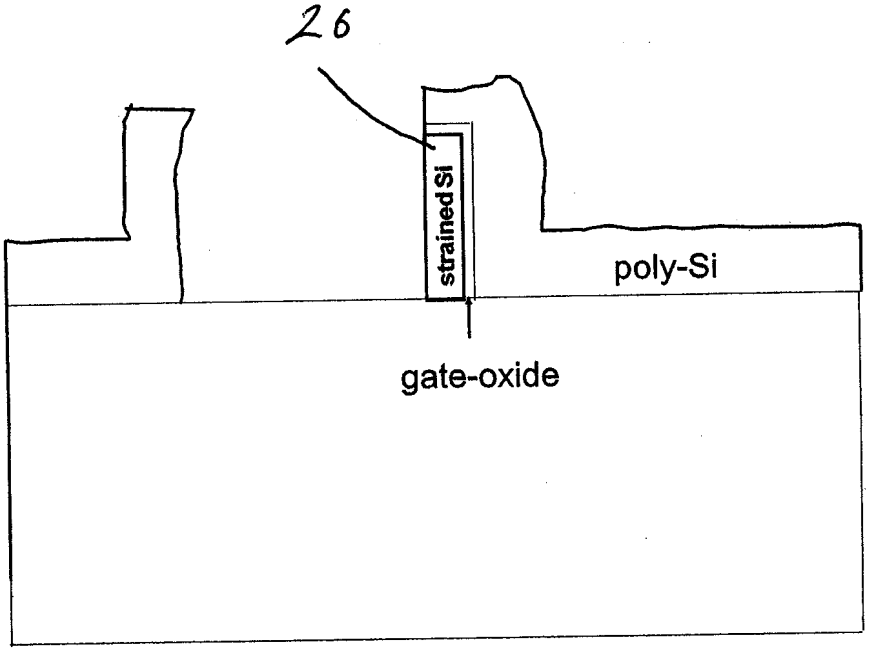
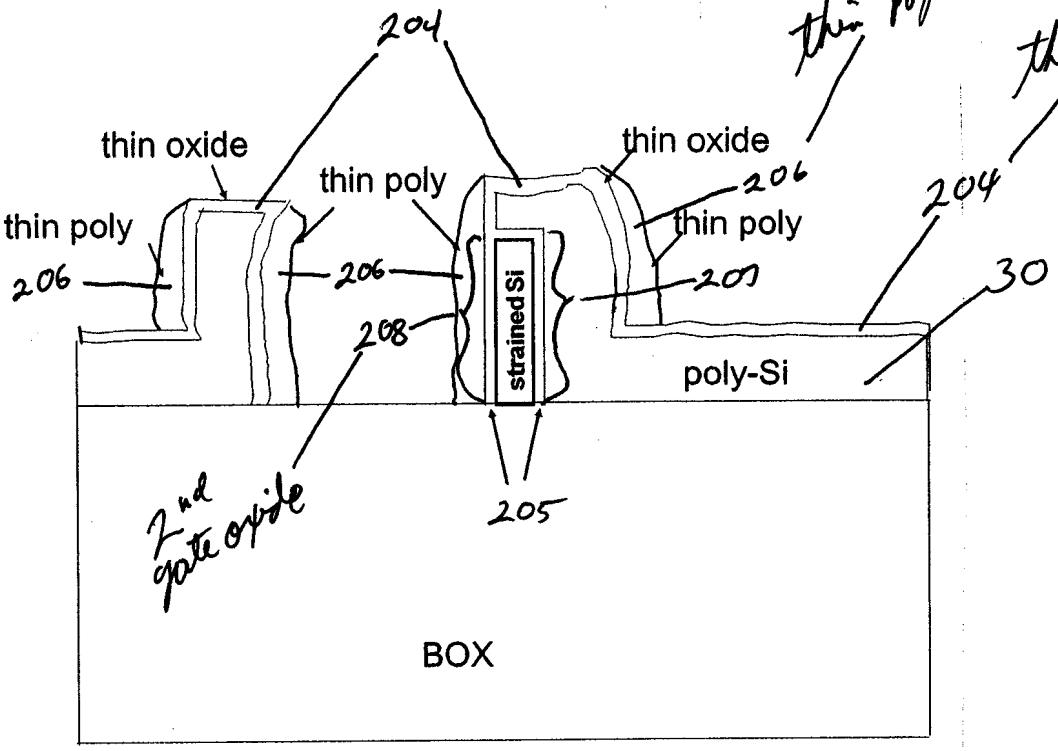


Figure18



3rd polysilicon layer

Figure 19